

REMARKS

Claims 1-10 are cancelled without prejudice or disclaimer to the subject matter recited therein. New claims 11-24 are added herein.

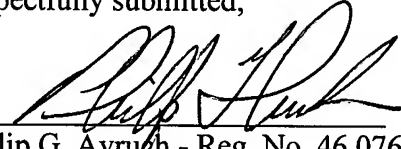
In the Final Office Action in parent application, dated April 15, 2003, the Examiner rejected all pending claims under 35 U.S.C. §102(b) as being anticipated by the Applicant's admitted prior art (AAPA), shown in Figure 4 the application. In a method according to the present claims, a first semiconductor chip is prepared having a semiconductor substrate area that does not contribute to circuit operation. For example, either the semiconductor substrate area is formed without transistors, or the area is formed with a memory that is not used, while a second chip has a second memory that is used instead. The second semiconductor chip is mounted just above the semiconductor substrate area. Thus, the semiconductor device according to the present invention has the advantage, as described in the application, of reducing the rise in temperature of the semiconductor device overall.

It is respectfully submitted that contrary to the Examiner's position, the AAPA fails to disclose a first semiconductor chip 403 having a semiconductor substrate area that does not contribute to circuit operation, and that a second semiconductor chip 405 is mounted just above the semiconductor substrate area of the first chip, as the claims require.

Please enter the Preliminary Amendment prior to calculating the filing fee.
Examination of the amended application is respectfully requested.

Respectfully submitted,

July 15, 2003
Date


Phillip G. Avrukh - Reg. No. 46,076
RABIN & BERDO, P.C.
Telephone: 202-371-8976
Telefax: 202-408-0924
E-mail : firm@rabinchamp.com
CUSTOMER NO. 23995

PGA:tlc